Analytical Delay Model for Distributed On-Chip RLCG Global Interconnects for Different Pole Conditions

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***Abstract*— Fast delay estimation methods, as compared to simulation techniques, are needed for incremental performance-driven layout synthesis. On-chip inductive and conductive effects are becoming predominant in deep submicron (DSM) interconnects due to increasing clock speeds; circuit complexity and interconnect lengths. Inductance causes noise in the signal waveforms, which can adversely affect the performance of the circuit and signal integrity. Elmore delay-based estimation methods, although efficient, fails to accurately estimate the delay for RLCG interconnect lines. This paper presents an analytical delay model, based on first and second moments of RLCG interconnection lines, that considers the effect of inductance and conductance for the estimation of delay in interconnection lines. Simulation results justify the efficacy of the proposed delay modelling approach.**

***Index Terms*— Moment, Delay calculation, Interconnect, RLCG, VLSI**

I. Introduction

With the development of ultra large scale integrated circuit (IC) process, interconnect delay is playing the dominant role as compared to the gate delay. Simple but effective analytical delay models of interconnects are useful for IC designers to avoid the timing issue problem and to optimize the design, such as minimizing delay [1-5]. Hence, it is necessary to build accurate and effective delay estimation models for interconnects. Elmore delay model [1], which is simple in form and easy to be used, has been widely adopted to estimate the interconnect delays in the performance-driven synthesis and layout of very large-scale integrated (VLSI) routing topologies. It is actually the first order estimation of the interconnect delay with an ideal step input signal, i.e., assuming rise time to be zero. Depending on the frequency used for circuit operation, topology of the interconnect structure, and the rise time of the input signal, the on-chip interconnect may be modelled either as lumped, distributed or as the full wave models. At relatively lower frequency, interconnect may be modelled as distributed RC segments [6-9]. In order to capture the high frequency effect such as, undershoot, overshoot, ringing, the interconnect is modelled as distributed RLC network [10-14] and the accuracy in performance estimation of interconnect eventually got improved. Unfortunately, these RC or RLC models lack in accuracy as the loss due to the dielectric component G can not be ignored in many practical situations especially in the very high frequency domain used in the present VLSI design [15]. With the increase in speed of high performance VLSI circuits, inductance and conductance effect of interconnects are becoming more and more important and can no longer be neglected. Under this circumstance, the Elmore model is inadequate since this model takes only the resistance and capacitance effects into account.

Nowadays, extensive methodologies and techniques are developed for the accurate estimation of the crosstalk noise and delay in DSM designs. Majority of them consider lumped and distributed RC or RLC interconnects. On-chip inductive effects are becoming predominant in deep submicron (DSM) interconnects due to increasing clock speeds; circuit complexity and decreasing interconnect lengths. Inductance causes noise in the signal waveforms, which can adversely affect the performance of the circuit and signal integrity. But, with increasing frequency range of operation, ignoring the effect of conductance can lead to degradation of the performance of the system. This inaccuracy can be harmful for performance driven routing methods which depend on the values of propagation delay. Generally in cases when high frequencies are considered (of the order of GHz), no dielectric can act like a perfect insulator (as taken to be ideally), thus there is always a probability of leakage, and conductance is considered as a measure of this leakage.

It is necessary to use a second order model, which includes the effect of inductance and conductance. There are several approaches proposed to estimate the on-chip interconnect performance characteristic; where the interconnect is modelled as distributed RLCG segment. In [16], the interconnect line is modelled as distributed RLCG elements and the frequency response is calculated and it is shown that RLCG consideration is suitable up to 110 GHz frequency of operation. Hua *et al.* [17] have proposed an interconnect RLCG state space models in time domain with computation complexity of O(N), where N is the total system order. An analytical delay model for distributed on-chip RLCG interconnects has been proposed in [18] taking step function as input. Another delay model proposed in [19] calculates delay of distributed RLCG interconnects by taking into

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consideration the coupling effect and by using difference model approach. In [20] also, the delay is calculated for on-chip global RLCG interconnect using step input. But these models suffer from accuracy point of view and no information regarding the damping conditions are provided.

In this paper, a novel analytical delay model for RLCG interconnects under step input is presented for different damping situations, i.e., over damped, under damped and critical damped cases. The rest of the paper is organized as follows: basic theory related to distributed RLCG interconnection network is discussed in section 2. In section 3, proposed delay model have been discussed for different types of poles and damping conditions. Simulation results are shown in section 4, while conclusions are made in section 5.

II. BASIC THEORY

The transfer function of a RLCG interconnect line with the source and load impedance as shown in Figure 1 can be obtained using ABCD parameters [21]. This is represented as:

$$H(s)=\frac{V_0(s)}{V_1(s)}=\frac{1}{\cos(Pd)\left(1+\frac{Z_S}{Z_T}\right)+\sinh(Pd)\left(\frac{Z_S}{Z_0}+\frac{Z_0}{Z_T}\right)} \quad (1)$$

where, $P=\sqrt{(r+sl)(g+sc)}$ is the propagation constant, Z_0 is the characteristic impedance for the RLGC interconnect.

$$Z_0=\sqrt{\frac{(R+sL)}{(G+sC)}} \quad (2)$$

where, $r=R/d$, $l=L/d$, $g=G/d$, $c=C/d$ are the values of resistance, inductance, conductance and capacitance per unit length and d is length of the interconnect. To compute the RLCG line response from the transfer function, the method of Padé approximation has been used by e.g. [22-23]. The output transfer function is expanded by Maclaurin series around s=0 and the series is terminated at the desired order. In general, the exact calculation of the voltage response is difficult and is usually not in closed form.

III. PROPOSED WORK

A simple closed form delay estimate is developed based on first and second moment, which considers the effect of inductance and conductance. The interconnect line is modelled arbitrarily and the source is considered as an inductor and a resistor in series. The interconnect comprises of RLCG segments. The load at the end of the interconnect comprises of a capacitor.

Thus, the source impedance

$$Z_S=R_s+sL_s$$

The characteristic impedance for the RLCG interconnect is

$$Z_0=\sqrt{\frac{(R+sL)}{(G+sC)}}$$

The load impedance $Z_L=\frac{1}{sC_T}$

The propagation constant for d length of the interconnect is given by

$$Pd=\sqrt{(R+sL)(G+sC)} \quad (3)$$

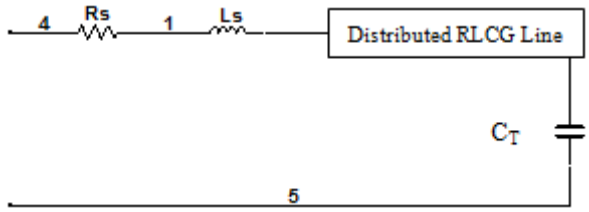

Figure 1. Modelled RLCG System

The hyperbolic function of the transfer function is expanded around s=0, and the terms only up to the coefficient of s^2 are considered. Hence, the transfer function reduces to the form:

$$H(s)\approx\frac{1}{(1+bs+cs^2)} \quad (4)$$

where,

$$b=(LG+RC)\left(\frac{1}{2!}+\frac{2RG}{4!}-\frac{R_SG}{3!}\right)+R_SC_T\left(1+\frac{RG}{2!}+\frac{R^2G^2}{4!}\right)+(L_SG+R_SC+RC_T)\left(1-\frac{RG}{3!}\right) \quad (5)$$

$$c=\left(\frac{LC}{2!}\right)+\left(\frac{L^2G^2+4RLGC+R^2C^2}{4!}\right)+(LG+RC)\left\{R_SC_T\left(\frac{1}{2!}+\frac{2RG}{4!}\right)-\frac{(L_SG+R_SC+RC_T)}{3!}\right\}+L_SC_T\left(1+\frac{RG}{2!}+\frac{R^2G^2}{4!}\right)+LC_T-\frac{1}{3!}\{LG(CR_S+C_TR)\} \quad (6)$$

The first and the second moment of the functions may be represented as:

$$M_1=b; \quad (7)$$

$$M_2=b^2-c \quad (8)$$

Depending on the sign of the moments of the transfer function, the poles can be real, or complex. In this paper, three different poles are considered in order to accurately capture the interconnect delay for different damping conditions.

A Real Poles

For the case of real poles, condition to be satisfied is

$b^2-4c>0$

The output voltage response will be of the form:

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$$v(t) = V_0\left(1 - \frac{s_2}{s_2 - s_1}e^{s_1 t} + \frac{s_1}{s_2 - s_1}e^{s_2 t}\right) \quad (9)$$

where,

$$s_2 = \frac{-b - \sqrt{b^2 - 4c}}{2c} \quad (10)$$

$$s_1 = \frac{-b + \sqrt{b^2 - 4c}}{2c} \quad (11)$$

$s_2 - s_1 = \frac{-\sqrt{b^2 - 4c}}{c}$ is negative and thus the factors $\frac{s_1}{s_2 - s_1}$ and $\frac{s_2}{s_2 - s_1}$ are positive.

As observed from the above equations,
abs(S_2) > abs(S_1), the third term in the voltage response can be ignored in comparison to the other terms, and thus the voltage response reduces to

$$v(t) = V_0\left(1 - \frac{s_2}{s_2 - s_1}e^{s_1 t}\right) \quad (12)$$

Since the voltage is lower bound, the delay obtained is an upper bound on the actual delay. The delay at a threshold voltage v_{TH} can then be obtained as

$$s_1\tau_r = \ln\left((s_2 - s_1)(1 - v_{TH})/s_2\right) \quad (13)$$

From equations (10-11) and (13), τ_r can be written as,

$$\tau_r = \frac{\ln\left(\frac{-2\sqrt{b^2 - 4c}(1 - v_{TH})}{-b - \sqrt{b^2 - 4c}}\right)}{\frac{-b + \sqrt{b^2 - 4c}}{2c}} \quad (14)$$

B. Complex Poles

For the case of complex poles, condition to be satisfied is

$$b^2 - 4c < 0$$

The time domain response will be of the form [24]:

$$\mathrm{v(t)} = \mathrm{v_0}\left(1 - \frac{\sqrt{\alpha^2 + \beta^2}}{\beta}e^{-\alpha t}\sin(\beta t + \rho)\right) \quad (15)$$

where $\alpha = \frac{M_1}{2\left(M_1^2 - M_2\right)}$ (16)

$$\beta = \frac{\sqrt{3M_1^2 - 4M_2}}{2\left(M_1^2 - M_2\right)} \quad (17)$$

$$\rho = \tan^{-1}\frac{\beta}{\alpha} \quad (18)$$

Using the above equation and the threshold voltage V_{TH}, it can be derived as,

$$e^{-\alpha t}\sin(\beta t + \rho) = \frac{(1 - v_{TH})}{\sqrt{1 + \frac{\alpha^2}{\beta^2}}} \quad (19)$$

This equation may be solved recursively to provide

$$\tau_c = \frac{\frac{(1 - v_{TH})e^{\alpha T_{ED}}}{\sqrt{1 + \frac{\alpha^2}{\beta^2}}} - \rho}{\beta} \quad (20)$$

From (7-8), (16-17), (18), (20), we can write

$$\tau_c = \frac{\frac{(1 - v_{TH})e^{\alpha T_{ED}}}{\sqrt{1 + \left(\frac{b^4}{3b^4 - 4b^2 + 4c}\right)}} - \tan^{-1}\left(\frac{\sqrt{3b^4 - 4b^2 + 4c}}{b^2}\right)}{\frac{\sqrt{3b^4 - 4b^2 + 4c}}{2\left(b^4 - b^2 + c\right)}} \quad (21)$$

where, T_{ED}= Elmore delay

C. Double Poles

For the case of complex poles, condition to be satisfied is $b^2 - 4c = 0$.

The output response will be of the form [24]:

$$v(t) = V_0\left(1 - e^{ts_1} - \frac{2te^{ts_1}}{b_1}\right)$$

$$V(s) = \frac{V_0}{sc\left(s - s_1^2\right)}\text{; where } s_1 = -\frac{b}{2c}$$

$$V(s) = V_0\left(\frac{1}{s} - \frac{1}{(s - s_1)} - \frac{2}{b_1(s - s_1)^2}\right)$$

Thus, the time domain response would be:

$$v(t) = V_0\left(1 - e^{ts_1} - \frac{2t}{b_1}e^{ts_1}\right) \quad (22)$$

We may calculate the time delay at some value of threshold voltage. But as already discussed in [24], this case rarely occurs. Hence we ignore it. Equations (14) and (21-22) show the proposed models for the calculation of delay for the distributed on-chip global RLCG interconnects for different pole conditions.

IV. Simulation Results and Discussions

The configuration of circuit for simulation is shown in Figure 1. We now develop a simple closed-form delay estimate, based on first and second moments, which to our knowledge is the first analytical delay model that handles arbitrary threshold voltages and inductance effects for a distributed line. The high-speed interconnect system consist of two coupled interconnect lines and ground and the length of the lines is d =100 um. The extracted values for the parameters R, L, C, and G are given in Table 1. Extraction

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process for the values of the parameters R, L,C, and G have been derived in [25].

TABLE I.
RLCG PARAMETERS FOR A MINIMUM- SIZED WIRES IN A 0.18µM TECHNOLOGY

Parameter(s)	Value/m
Resistance(R)	120 kΩ/m
Inductance(L)	270 nH/m
Conductance(G)	15f pS/m
Capacitance(C)	240 pF/m

Table-2 shows the comparative result of the delay for different values of source elements like Rs, Ls, and output capacitance C_T computed using SPICE and the proposed method when the poles are real. Table2 also shows that for higher values of the source resistor, the accuracy of the proposed delay model increases, e.g. for Rs=2kΩ, the proposed delay model results in an error of as low as 0.62% compared to that of the SPICE delay.

TABLE I.
COMPARISON OF THE DELAY COMPUTED USING SPICE WITH PROPOSED MODEL WHEN POLES ARE REAL

Rs (Ω)	Ls (pH)	C_T (pF)	Spice Delay (ps)	New Model (ps)	% Error
50	2.46	0.176	24.33	21.67	-10.93
100	2.46	0.176	47.30	46.32	-2.07
500	2.46	0.176	214.50	223.78	4.33
1000	2.46	0.176	456.20	441.98	-3.11
2000	2.46	0.176	897.68	892.13	-0.62

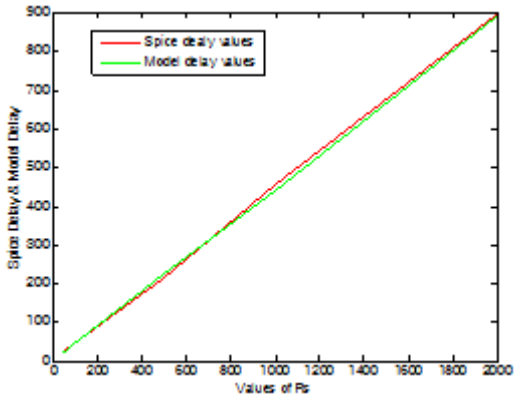

Figure 2. Comparison of the SPICE with the proposed delay model (in ns) for real poles when Ls= 2.46pH, C_T=0.176pF

Table-3 shows the comparative result of the delay for different values of source elements like Rs, Ls, and output capacitance C_T computed using SPICE and the proposed method when the poles are complex. Table 3 also shows that in case of complex poles the proposed delay model results in error as low as 1.4% compared to that of the SPICE simulations.

TABLE I.
COMPARISON OF THE DELAY COMPUTED USING SPICE WITH PROPOSED MODEL WHEN POLES ARE COMPLEX

Rs (Ω)	Ls (pH)	C_T (pF)	Spice Delay (ps)	New Model (ps)	%Error
10	0.0246	0.0176	1.32	1.35	2.27
15	0.0246	0.0176	1.43	1.45	1.4
20	0.0246	0.0176	1.58	1.62	2.53
25	0.0246	0.0176	1.65	1.68	1.82

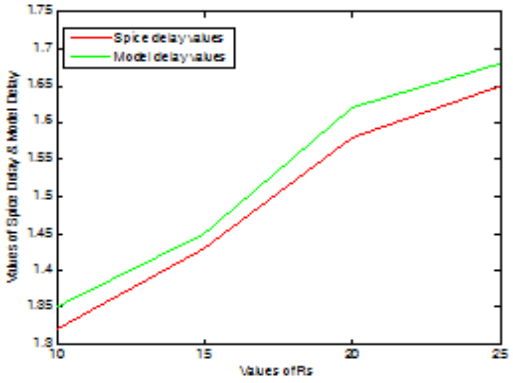

Figure 3. Comparison of the SPICE with the proposed delay model (in ns) for complex poles when Ls=0.02466pH, C_T= 0.0176pF

We can calculate the time delay at some value of threshold voltage for the condition for double poles. But this case rarely occurs [24]. Hence we ignore it.

V. CONCLUSIONS

The paper presents an analytical delay model, based on first and second moments of RLCG interconnection lines, which considers the effect of inductance. The resulting delay estimates are significantly more accurate. The derived expression along with this analysis can serve as a convenient tool for delay estimation without much computation during design. Simulation results demonstrate the validity and correctness of the proposed method.

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